REMARKS

This Response responds to the Office Action dated February 3, 2005 in which the Examiner rejected claim 3 under 35 U.S.C. §102(e), objected to claim 4 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form and stated that claims 5 and 6 are allowable over the prior art of record.

Claim 3 claims a trace control circuit comprising an address capturing means, a data capturing means and an output means. The address capturing means captures a relative address in a memory access by a CPU. The data capturing means captures access data of the CPU. The output means outputs a reference address to a trace bus and outputs the relative address in the memory captured by the address capturing means and the access data captured by the data capturing means.

Through the structure of the claimed invention a) capturing a relative address and access data and b) outputting a reference address, the relative address and access data as claimed in claim 3. the claimed invention provides a trace control circuit in which the number of cycles required to output the event of the access instruction is reduced without increasing the number of DATA terminals and the capacity of the trace memory. The prior art does not show, teach or suggest the invention as claimed in claim 3.

Claim 3 was rejected under 35 U.S.C. §102(e) as being anticipated by *Edwards et al* (U.S. Patent No. 6,615,370).

Applicant respectfully traverses the Examiner's rejection of the claim under 35 U.S.C. §102(e). The claim has been reviewed in light of the Office Action, and for

reasons which will be set forth below, applicant respectfully requests the Examiner withdraws the rejection to the claim and allows the claim to issue.

Edwards et al appears to disclose performing trace on a system-on-chip (SOC), and more specifically, to storing trace information. (col. 1, lines 8-10) A non-intrusive trace system receives trace information from one or more processors or other devices. The trace system may include a first-in, first-out (FIFO) buffer which stores trace information. In one embodiment, the FIFO buffer is memory-mapped and is capable of being accessed by other systems without affecting processor performance. In one aspect of the invention, the trace system includes a trace buffer which receives information at an internal clock speed of the processor. (col. 2, lines 10-20) Further, the trace information collected includes all of the information needed to perform trace operations; the processor does not need to be interrupted to obtain additional information, such as by a software program running on a debug tool. (col. 2, lines 26-30) In one embodiment, the trace information includes both address information and message information. In another aspect, the trace information includes timing information. In one aspect, the trace system may be used as a rate converter for converting a transmission rate of messages transmitted to a memory system on-chip or an external system. (col. 2, lines 33-39) In another aspect, the trace information may be compressed by the trace system. (col. 2, lines 40-41) Also, information may be filtered by predefining criteria upon which trace information is generated. (col. 2, lines 49-50)

Thus, *Edwards* merely discloses collecting trace information including both address information, message information and timing information. However, nothing in *Edwards et al* shows, teaches or suggests a) capturing a relative address, b)

capturing access data and c) outputting a reference address, relative address and access data as claimed in claim 3. Rather, *Edwards et al* merely discloses collecting trace information including address information, message information and timing information.

Since nothing in *Edwards et al* shows, teaches or suggests a) capturing a relative address, b) capturing access data and c) outputting a reference address, relative address and access data as claimed in claim 3, applicant respectfully requests the Examiner withdraws the rejection to claim 3 under 35 U.S.C. §102(e).

Since objected to claim 4 depends from an allowable claim, applicant respectfully requests the Examiner withdraws the objection thereto.

The prior art of record, which is not relied upon, is acknowledged. The reference taken singularly or in combination does not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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